REMARKS

Applicant respectfully requests reconsideration of the present application in view of the foregoing amendments and in view of the reasons that follow.

Status of Claims:

No claims are currently being cancelled.

Claims 1, 2, 5-9, 12-15 and 17-20 are currently being amended.

Claim 21 is currently being added.

This amendment and reply amends and adds claims in this application. A detailed listing of all claims that are, or were, in the application, irrespective of whether the claims remain under examination in the application, is presented, with an appropriate defined status identifier.

After amending and adding the claims as set forth above, 1-21 are now pending in this application.

Claim Rejections – 35 U.S.C. § 101:

In the Office Action, claims 1-20 were rejected under 35 U.S.C. § 101 as being to non-statutory subject matter, for the reasons set forth on pages 2 and 3 of the Office Action. By way of this amendment and reply, the preamble of the 'computer' claims have been amended in the manner suggested in the Office Action, and each of the presently pending independent claims has been amended to recite "useful, concrete and tangible" results.

Accordingly, all of the presently pending claims are believed to fully comply with 35 U.S.C. § 101.

Claim Rejections – Prior Art:

In the Office Action, claims 1-20 were rejected under 35 U.S.C. § 102(e) as being anticipated by "Applied Boolean Equivalence Verification and RTL Static Sign-Off", by Harry Foster; claims 1-20 were rejected under 35 U.S.C. § 102(b) as being anticipated by "As good as gold", by Blackett; and claims 1-20 were rejected under 35 U.S.C. § 102(b) as being anticipated by "On the Formal Verification of ATM Switches", by Jianping Lu. These rejections are traversed with respect to the presently pending claims under rejection, for at least the reasons given below.

Presently pending independent claim 5 recites, among other things:

a storage section for storing an object code compiled from an behavioral level description written in a programming language, the object code being used for specification verification by simulation on a CPU in a design phase,

an RT level description generated from the behavioral level description,

correspondence information which specifies information on pairs of fragments of descriptions to be compared which are included in the behavioral level description and the RT level description and which specifies information on pairs of signals to be compared for each description pair, and

compile information including mapping information between the behavioral level description and the object code;

a first logic cone extraction section for extracting first logic cones of variables by:

searching a code portion and the variables of the object code corresponding to each fragments of descriptions and each signals of behavioral level description to be compared which are specified by the correspondence information by referencing the compile information,

setting initial symbol values in the variables,

performing symbolic simulation from the start to end points of the code portion to produce symbol values when the variable symbolic simulation ends, and

using the symbol values as the first logic cones of the variables;

a second logic cone extraction section for extracting second logic cones each for the signals for each fragments of description of RT level description to be compared which are specified by the correspondence information; and

a logic cone comparison section for comparing the first logic cones and the second logic cones for each signals for each of the fragments of descriptions to be compared in the behavioral level description and the RT level description which are specified by the correspondence information.

wherein, based on the comparison of the first logic cones and the second logic cones, a determination is made as to whether the RT level description that has been designed in a behavioral synthesis phase is acceptable to be used in a manufacturing phase for the logic circuits.

The above features of claim 5 are not disclosed or suggested by any of the cited art of record. Namely, Foster is directed to transforming a high-level model representation of a design into a physical transformation, whereby no comparison of *first logic cones and second logic cones is made so as to determine whether the logic circuits that have been designed in a design phase are acceptable to be used in a manufacturing phase for the logic circuits.*

Blackett is directed to logic simulation for performing functional verification, whereby no comparison of *first logic cones and second logic cones is made so as to determine whether the logic circuits that have been designed in a design phase are acceptable to be used in a manufacturing phase for the logic circuits*.

Jianping Lu is directed to formal verification of ATM switches used in simulating large digital designs, whereby no comparison of *first logic cones and second logic cones is made so as to determine whether the logic circuits that have been designed in a design phase are acceptable to be used in a manufacturing phase for the logic circuits*.

Accordingly, presently pending independent claim 5 is not anticipated by any of the cited art of record.

Presently pending independent claims 1, 2, 6, 8, 13, 15 and 19 recite similar features to those highlighted above with respect to claim 5, whereby those independent claims are also not anticipated by the cited art of record.

Presently pending independent claim 7 recites, among other things:

a symbolic simulation section which, by referencing the compile information, searches a code portion and variables of the object code corresponding to logic cone extraction areas and signals to be extracted which are specified by the correspondence information, sets initial symbol values in the variables, and performs symbolic simulation from the start to end points of the code portion; and

an output section for outputting symbol values which are obtained when the variable symbolic simulation ends, as logic cones of the variables,

wherein, based on the logic cones of the variables, a determination is made as to whether the logic circuits that have been the object code being used for specification verification by simulation on a CPU in a design phase.

Such features as provided above in presently pending independent claim 7 are not disclosed or suggested by any of the cited art of record.

Presently pending independent claim 17 recites, among other things:

wherein a step of extracting first logic cones comprises the steps of:

b.1) searching a code portion and the variables of the object code corresponding to each fragments of description and each signals of behavioral level description to be compared which are specified by the correspondence information by referencing the compile information;

b.2) setting initial symbol values in the variables;

b.3) performing symbolic simulation from the start to end points of the code portion; and

b.4) determining the first logic cones of the variables as symbol values when the variable symbolic simulation ends.

Such features as provided above in presently pending independent claim 17 are not disclosed or suggested by any of the cited art of record. In more detail, none of the cited art of record discloses or suggest such steps involved in extracting first logic cones. The fact that these references disclose the use of logic cones, by itself, falls well short of the specific features recited in presently pending independent claim 17.

In a similar manner, each of the other presently pending independent claims are not anticipated by the cited art of record.

New Claim:

New claim 21 has been added to recite features seen best in Figure 4 of the drawings and as described in the specification, whereby such features are believed to patentably distinguish over the cited art of record, when taken as a whole.

Conclusion:

Since all of the issues raised in the Office Action have been addressed in this Amendment and Reply, Applicant believes that the present application is now in condition for allowance, and an early indication of allowance is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check or credit card payment form being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741. If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicant hereby petitions for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 19-0741.

Respectfully submitted,

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